



Startup Voltage Tracking With MSK5910RH and 5922RH Low Dropout Radiation Hardened Regulators

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The MSK5910RH and MSK5922RH are 5A, radiation hardened, low dropout regulators with input to output voltage tracking capability. Many FPGAs require a logic power supply that is greater than the core voltage. Additionally the logic power supply often cannot exceed the core voltage by a predetermined margin during startup. These regulators allow the output voltage to track the input voltage up to the regulation set point where the output levels off and the input continues to rise to its final value. This feature allows the MSK5910RH and MSK5922RH to meet the unique power-up requirements of many FPGAs and logic devices.

Operation

The Vbias pin provides power to all of the control circuitry for the MSK5910RH and MSK5922RH. Vin is the input voltage source that will be regulated down to the output voltage set point. Providing power to the Vbias pin before providing power to the Vin pin(s) forces the control circuitry to try to saturate the pass transistor. In this state the pass transistor will fully saturate as soon as the input voltage exceeds the VBE potential of approximately 0.7V and the output will track the input as $V_{in} - V_{CE(SAT)}$. Hard saturation of the pass transistor is interpreted as a fault condition by the controller and the fault latch will begin to charge. Holding the latch pin low during startup disables the fault latch and prevents the latch circuit from disabling the regulator. The latch pin can be held low for startup only or indefinitely and only sources approximately 7uA during a fault condition.

Fault Latch Operation - Disabling and Enabling

The fault latch disables the regulator by charging a user-selected capacitor with a nominal 7uA current source whenever the pass transistor drive circuit saturates. The device will latch off once the latch capacitor voltage reaches 1.4V typical. Under normal operation this feature allows the regulator to source higher than normal current surges that may be required during startup or recovering from an idle state to a fully active state. The time delay from overload to latch is a function of the user selected latch capacitor and is approximated by the equation $t = 200 * 10^3 * C_{latch}$. The latch can be reset by pulsing the latch pin low to discharge the latch capacitor and disabled by holding the latch pin low. The latch can also be reset by cycling power on both the MSK5922RH and the MSK5910RH or toggling the shutdown pin on the MSK5910RH. Input to output voltage tracking at startup is accomplished by holding the latch pin low during startup to disable the latch. The latch pin can be tied directly to ground if the latch feature is not desired

during normal operation or released after start up to enable the latch feature. A simple transistor circuit can be configured to control the latch. Refer to the figures below for example circuits that can easily be tailored for a variety of specific applications. Refer to the product data sheets on the RAD HARD PRODUCTS section of the MSK website for additional applications information.

<http://www.mskennedy.com/store.asp?pid=9951&catid=19680>

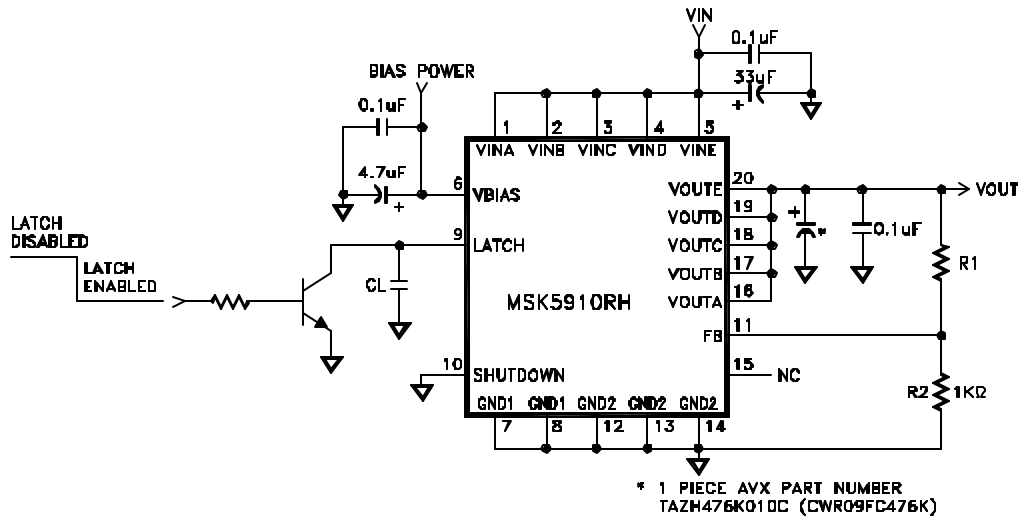


Figure 1

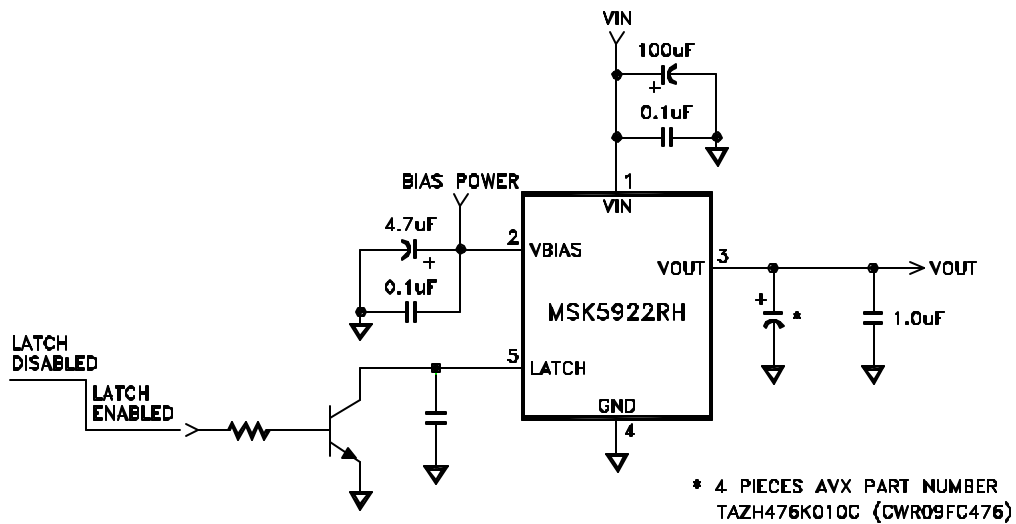


Figure 2

Typical Startup Waveforms

The waveforms below demonstrate the typical input to output tracking of a 2.5V device driving a 3A resistive load with differing input ramp rates.



Figure 3

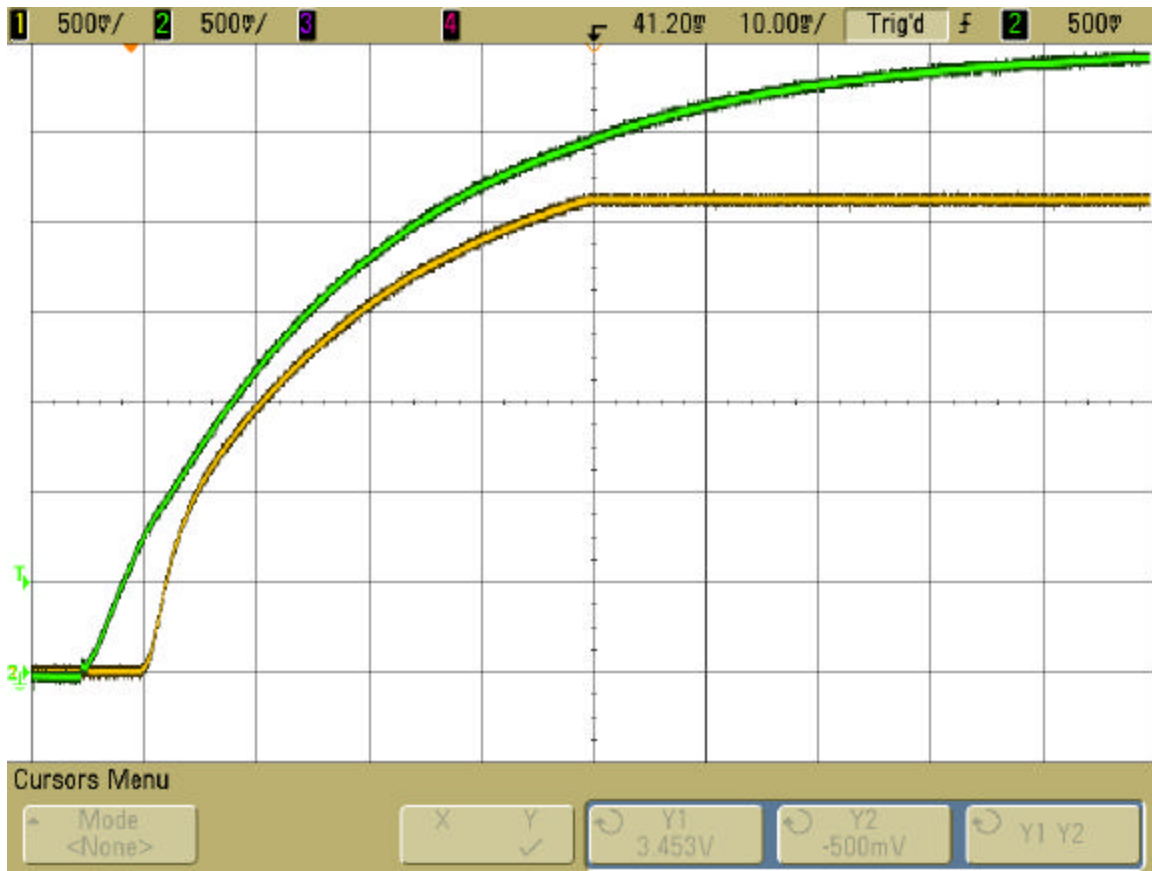


Figure 4

Summary

The MSK5910RH and MSK5922RH regulators are well suited for the demanding startup requirements of modern FPGAs and logic devices. Input to output voltage tracking, increased startup current capacity and high momentary surge current capacity all cater to the needs of these demanding logic devices.