



High Efficiency Point of Load Regulation With MSK504X series switching regulators, MSK5040, 5041, 5042, 5043, 5045

By Paul Musil, MS Kennedy Corp.; 04/2007
Revised 07/26/2007

The MSK504X series are high efficiency synchronous rectified switching regulators. These regulators were designed to provide very efficient POL (Point Of Load) regulation for a variety of low voltage applications including Microprocessors, FPGAs etc... With a minimum input voltage of 4.5V they are well suited for converting a 5V power bus down for lower voltage logic devices. Output current capabilities of up to 8A make these regulators a good choice for powering today's high power CPUs and FPGAs. The absolute maximum input is 30V for the MSK5040, 41, 42, 43 and 80V for the MSK5045 allowing usage in a wide variety of applications with higher bus voltages. The MSK504X series switching regulators can provide very tight regulation when proper component selection and board layout are adhered to. The MSK504X series require only three external component selections and a proper circuit board layout for optimal performance. This note will explain the how and why for each.

Sense Resistor Selection

Proper selection of the sense resistor (RS) will aid in configuring a problem free circuit. Low inductance resistors, such as surface metal film type, are preferred. The voltage across RS is used to limit the maximum output current, provide a current mode control signal and change operating modes to improve efficiency at light loads. During normal operation the RS current is a triangle wave riding on a DC offset with an average value equal to the DC load current. RS converts the current waveform to a voltage waveform and feeds it back to the controller. The controller compares the current in RS to the current demand that is derived from the voltage feedback to maintain regulation of the output. If the signal across RS exceeds the over-current threshold of 100mV (+20%) the controller will terminate the drive signal to the upper MOSFET thereby limiting the duty cycle and the maximum output current. If the signal across RS falls below 30mV (+20%), the controller will begin to skip drive pulses to reduce the switching frequency thereby reducing switching and gate losses in the power MOSFETs. Pulse skipping mode can be disabled in the MSK5045 by leaving the PWR SAVE pin open circuit. If the signal across RS falls through zero, the synchronous rectifier is immediately turned off to prevent discharging the output capacitors and further improves efficiency. In some configurations the output regulation may vary more widely as the device changes modes of operation giving the appearance of increased line and load regulation error. Keeping the signal fed back from RS noise free and within the correct range for the desired operating mode will ensure solid and stable regulation of the output.

Three parameters are needed to determine the correct value for RS; typical output current, maximum output current and AC output ripple current. The typical and maximum output current levels will be defined in the application specifications. The AC ripple current is calculated using the following formula:

$$I_{pp} = \frac{(V_{in} - V_{out} - I_{out} * R_x) * (V_{out} + I_{out} * R_x)}{V_{in} * L * 300\text{KHz}} \quad (\text{Amps p-p})$$

Given:

V_{in} = input voltage

V_{out} = output voltage

I_{out} = output current

R_x = 0.100 ohms

L = 2.35uH (MSK5040, 5041); 6.4uH (MSK5042, 5045); 3.3uH (MSK5043)

The most critical part of selecting a value for RS is to guarantee the maximum load can be supported. The output current is limited when the RS signal exceeds 100mV (+-20%), (80 to 120mV). Set the maximum value of RS with the following formula

$$R_{S_{max}} = \frac{80\text{mV}}{I_{out_{max}} + \frac{1}{2} I_{pp}} \quad (\text{ohms})$$

Given:

$I_{out_{max}}$ = the maximum required load current

This value may need to be lowered somewhat to provide additional margin, account for component tolerances and prevent noise from tripping the over-current latch. The adjusted value will ensure the design is capable of providing the maximum desired load current plus some margin. In some noisier systems a small RC filter is placed in the RS feedback to remove high frequency noise. If filtering is required, placing a 4700pF between pins 2 and 3 as close to the device as possible with a 22-ohm resistor in series between pin 2 and the sense resistor typically provides adequate high frequency noise reduction.

Analysis of the RS value will determine the expected modes of operation. The combined DC + AC feedback to the controller is calculated with the following formula:

$$V_{RS} = R_S * (I_{out} + \frac{1}{2} I_{pp})$$

Repeat the formula for $I_{out} = I_{out_{max}}$ and $I_{out} = I_{out_{typ}}$

If the maximum value exceeds the current limit threshold, the controller will limit the output current and the output voltage will decrease. If the minimum value goes below the lower threshold the controller will assume a very light load and begin skipping drive pulses to save on switching and gate drive losses. Under some operating conditions the peak-to-peak ripple current is too great to keep the RS feedback under the current limit

and in full PWM mode (above the pulse skipping threshold). In many circuits this is not a problem as long as the maximum load current can be delivered. Ipp can be reduced if the system is sensitive to the device changing operating modes.

To reduce Ipp the designer can increase L in the formula above. Placing an additional inductor at the output of the device adds directly to the internal inductance. When selecting an inductor for the application it is important to ensure it is well suited for high frequency switching regulators, has very low DC resistance and is designed for the expected load current. The peak-to-peak current ripple should not be reduced below 20% of the maximum expected load current. The formula below will determine the ideal amount of additional inductance required for a given application.

$$L_{ext} = \frac{(V_{in} - V_{out} - I_{out} * R_x) * (V_{out} + I_{out} * R_x)}{V_{in} * I_{pp} * 300KHz} - L$$

Given:

L_{ext} = external inductance to be added

Ipp = desired peak to peak current ripple

Typically $0.20 I_{out_{max}} \leq I_{pp} \leq 0.40 I_{out_{max}}$

Output Capacitor Selection

Use only low ESR capacitors intended for use in switching regulator applications. AVX TPS series, Sprague 595D series, Sanyo OS-CON, Nichon PL series, and Kemet T510 series capacitors typically work well. The total capacitance and ESR must meet the inequalities below for maximum performance.

$$C > \frac{2.5 * (1 + V_{out}/V_{in_{min}})}{V_{out} * R_S * 300KHz}$$

$$ESR < \frac{R_S * V_{out}}{2.5V}$$

These equations provide 45 degrees of phase margin to ensure stable fixed frequency operation and provide a damped output response to step load changes. Lower quality capacitors can be used if the load lacks step changes. Placing high frequency ceramic capacitors in parallel with the bulk capacitance and the load can further reduce high frequency switching noise. Bench testing over temperature is recommended to verify acceptable noise and transient performance.

The output ripple is usually dominated by the ESR of the output capacitors and can be approximated with the following equation:

$$V_{out_{ripple}} = I_{pp} * ESR$$

Including the capacitive term, the full equation for output ripple in continuous mode is shown below.

$$V_{out_ripple} = IPP * ESR + \frac{I_{pp}}{2 * \pi * 300KHz * C}$$

In pulse skipping mode, the pulses become wider and the frequency is reduced. The equation to approximate output ripple in pulse skipping mode is shown below.

$$V_{out_ripple} = \frac{0.02 * ESR}{RS} + \frac{0.0003 * L * (1 / v_{out} * 1 / (V_{in} - V_{out}))}{RS^2 * C}$$

Input Capacitor Selection

The input capacitor must both minimize the reflected ripple seen by the input bus to meet system requirements and provide a low impedance input to the regulator. The switching regulator is a constant power device and consequently looks like negative impedance to the input bus. An increase in input voltage results in a decrease in input current. The DC resistance is approximated by dividing the input voltage by the input current. It can also be approximated from the output power and the efficiency as shown below.

$$Z_{inDC} = -V_{in} / I_{in}$$

$$Z_{inDC} = \frac{-V_{in}^2}{P_o / Eff}$$

Given:

V_{in} = Input Voltage

I_{in} = Input Current

P_o = Output Power

Eff = Efficiency Factor eg. use 0.90 for 90%

The input impedance of the switching regulator only appears negative at relatively low frequencies compared to the switching frequency; typically less than ¼ of the switching frequency. It is important to have the input bus impedance much lower than the regulators input impedance in the range where it appears negative to prevent oscillation between the input bus and the regulator. It is important to consider all cabling inductance and resistance when determining the input bus impedance, especially at high output power levels. At DC, the bus impedance is simply the resistance of the bus materials and cabling in series with the internal equivalent resistance of the power source. As frequency increases the inductance of the bus materials and equivalent AC impedance of the power source begin to dominate and the bus impedance seen by the switching regulator increases. Adding bulk input capacitance between the input pins and the ground pins of the regulator counters this effect. The bulk capacitance should be low ESR, aluminum electrolytic or tantalum. Care must be taken when using tantalum with robust power sources to prevent inrush current failures.

Low impedance at the switching frequency also helps to minimize the voltage ripple reflected from the switching action of the regulator. Excessive high frequency ripple can adversely affect regulation accuracy and stability. This can be minimized by placing between 1.0 and 10uF of high frequency ceramic capacitance between the Vin and Ground pins of the regulator. The exact requirement is difficult to specify without a thorough analysis of the input bus and the bulk capacitance. AWG #18 wire for example is approximately 386nH per foot resulting in an AC impedance of 0.727 ohm per foot at the 300KHZ switching frequency. A switching regulator operating at 4A output with no input capacitance would produce approximately 2.9Vpp of input ripple per foot of 18AWG wire in the supply and return line. The input to the regulator switches between zero amps and the output load current at 300KHz in continuous operation. The high frequency characteristics of the bulk capacitance and the input supply bus will determine how much of that switching current will be forced into the high frequency ceramic capacitance. Assuming 80 to 90% of the switching current ripple in the ceramic capacitance will usually give a conservative approximation; though a very low impedance bus with high quality bulk capacitance may carry a larger percentage of the high frequency current and require less ceramic capacitance.

$$Z_{Cin} = \frac{1}{2 * \pi * 300KHz * C_{in_{ceramic}}} \quad \text{Z at fundamental switching frequency}$$

$$Q_{sw} = \frac{I_{out} * V_{out}}{300KHz * V_{in}} \quad \text{Approximate charge draw of each pulse}$$

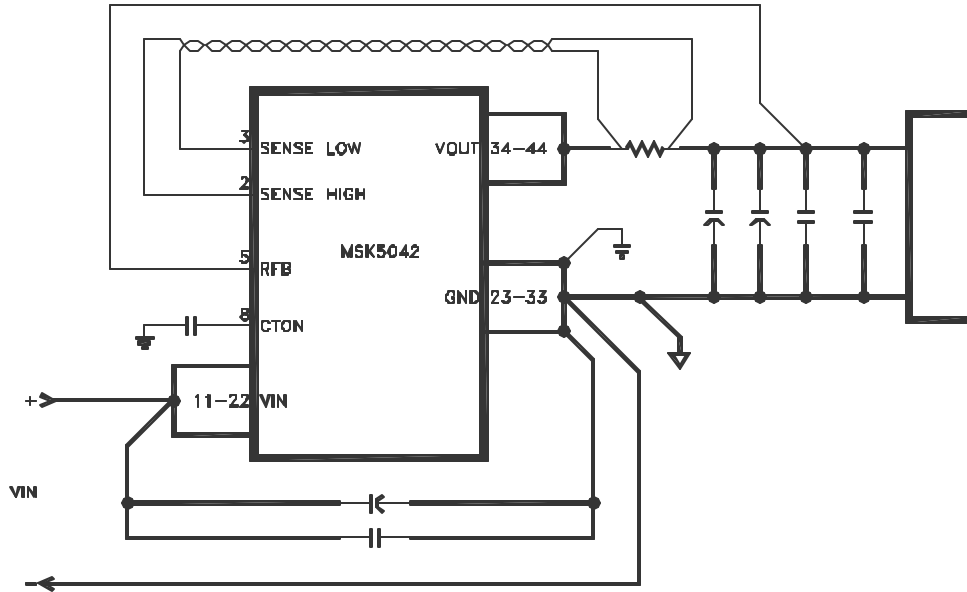
$$V_{pp}(Q) = \frac{Q_{sw} * (V_{in} - V_{out})}{V_{in} * C_{in_{ceramic}}}$$

The formulas above provide a reasonable approximation of the input voltage ripple at the switching frequency assuming 100% current in the ceramic capacitors and constant DC current in the input supply bus. Reduce the output current in the equations by the percentage assumed to be absorbed in the bulk capacitance and the input supply bus.

Layout of the Power Circuit

Proper layout of the power circuit is crucial to obtaining peak performance from any switching regulator. The circuit designer must remember that the ground current from the load returns to the input source when the forward power switch is in its on state and returns through the regulator ground pins when the switch is in its off state. This makes the return lines switch the full load current at 300KHz. To accommodate this the switching regulator return pins should be used as a single point star type ground with three primary power returns and one small signal return for control circuitry. The three power returns are; input power return, input capacitance, and the output load return. Keeping these three return lines on their own low impedance path will keep the ground noise to a minimum. Connect the input capacitance directly between the Vin pins and the Ground pins of the device. The output should have as short of a path as possible to RS

and from RS to the output bulk capacitance. RS should be connected with short connections to minimize noise pickup, twisted pairs work well for this connection. Feedback should also be connected with a very short direct connection. Reference the diagram below for power path layout.



- 1/ BOLD LINES INDICATE HIGH CURRENT AND SWITCHING CURRENTS. USE SHORT WIDE TRACES TO MINIMIZE IMPEDANCE.
- 2/ SEE PRODUCT DATA SHEETS FOR MORE PRODUCT SPECIFIC INFORMATION.

Summary

The MSK504X series offer a wide range of high efficiency solutions to meet a wide variety of demanding applications. Careful selection of supporting components tailors the devices to provide optimum performance in specific applications. The layout of the circuit board is critical to the performance of any switching regulator circuit. Following the layout guidelines for the MSK504X series will minimize noise and maximize performance. The guidelines presented above simplify the task of designing a problem free circuit with the MSK504X series of switching regulators.