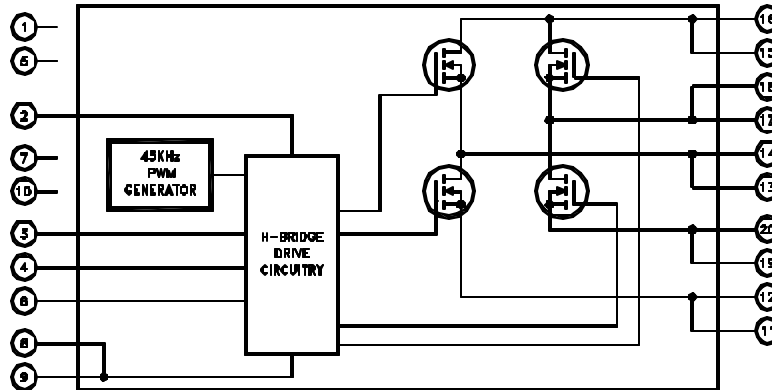


MSK4225 Closed Loop Controller

By Dan Williams, MS Kennedy Corp.; 09/2007

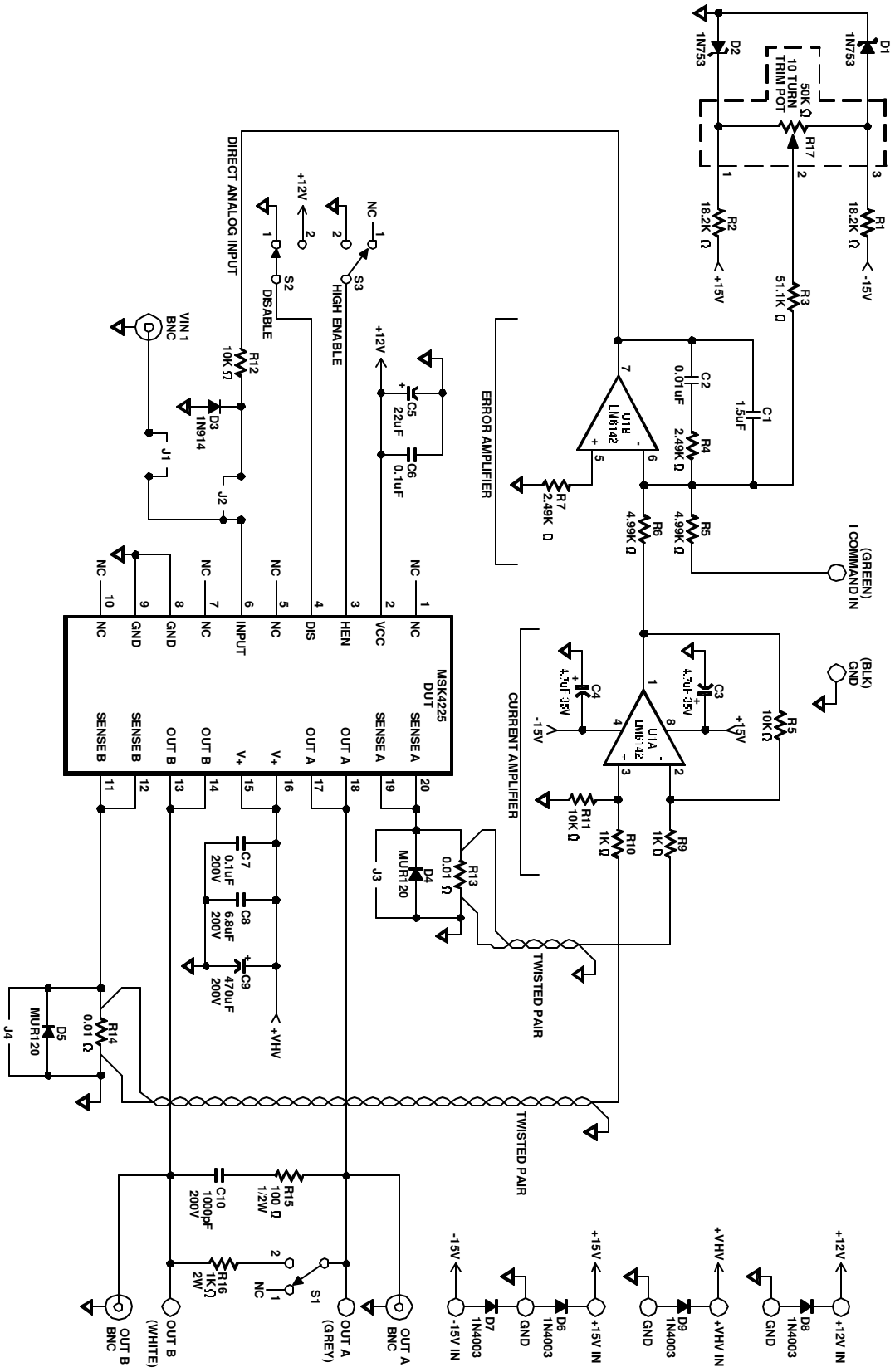
The MSK4225 is a MOSFET H bridge with internal gate drive and a PWM generator, all in one convenient package. This configuration can be used to control a variety of loads, such as a brushed DC motor or a voice coil. Because of the internal PWM generator, all the user needs to do is provide an analog voltage representative of the PWM duty cycle desired on the output.



The PWM scheme used in this device is referred to as complimentary modulation, or “locked anti-phase” modulation. In this modulation scheme, the analog input creates a PWM duty cycle extending from 100% (DC) in one direction to the load, all the way to 100% (DC) in the other direction. The middle is 50% modulation. In this configuration, 50% modulation creates zero average current through the load, even though current is being sent to the load in both directions. Since the current rise in one direction is exactly equal to the current rise in the other direction, the net is zero current.

The advantage in complementary modulation is that the PWM doesn’t stop as the controller goes through zero. Most controllers stop the PWM in one direction to produce zero current, and then start up PWM in the opposite direction. This creates a discontinuity in the control loop. Somewhere along the line, the controller has to make a decision to reverse the PWM. This cannot happen instantaneously and will disrupt the control when working the system near the zero current point, for instance, when an antenna is being steered ever so slowly to track a target. See “Torque Control vs. Speed Control” Application Note for more explanation of the PWM scheme involved in the MSK4225.

The evaluation card described in this note is set up to allow the user to operate the MSK4225 in a closed control loop scheme for controlling current through a load. Outside the MSK4225 are sense resistors that measure current through each leg of the H bridge. An amplifier sets up the resulting voltage waveform to be used in an error amplifier, also provided on the card. This amplifier compares the desired current command signal to the resulting current waveform and outputs this error level to the analog input of the MSK4225. Offset voltage adjustment is also provided on the card. Finally, all of the necessary bypassing and stability components are on-board to provide an ideal subsystem in which the MSK4225 can perform its function.



- NOTES:
1. ALL RESISTORS ARE 1/8W, ±1% UNLESS OTHERWISE SPECIFIED.
 2. ALL CAPACITORS ARE 35V MINIMUM, ±10% UNLESS OTHERWISE SPECIFIED.

Evaluation Card Parts List

R1, R2	18.2K	250mW	Dale RN55D1822F
R3	51.1K	250mW	Dale RN55D5112F
R4, R7	2.49K	250mW	Dale RN55D2491F
R5, R6	4.99K	250mW	Dale RN55D4491F
R8, R11, R12	10.0K	250mW	Dale RN55D1002F
R9, R10	1.0K	250mW	Dale RN55D1001F
R13, R14	0.010	10W	Isotek PBV-R010-1.0
R15	100	500mW	Clarostat RW70U1000F
R16	1.0K	2W	Dale RS-2B 1K? 1%
R17	50K/10	Turn Pot	Clarostat 364X 50K
C1	1.5uF		AVX SR505C155JAB
C2	0.01uF		Mallory CK06BX103K
C3, C4	4.7uF		Kemet T322D475K050AS
C5	22uF		Kemet T322E226K035AS
C6, C7	0.1uF		Mallory CK06BX104K
C8	6.8uF		Illinois Capacitor 685MWR250K
C9	460uF		Sprague 53D 460uF 200VDC
C10	1000pF		Mallory CK05BX102K
U1	LM6142		National LM6142AIN
D1, D2	1N753		Microsemi
D3	1N914		Fairchild Semiconductor
D4, D5	MUR120		On Semiconductor
D6 – D9	1N4003		Fairchild Semiconductor

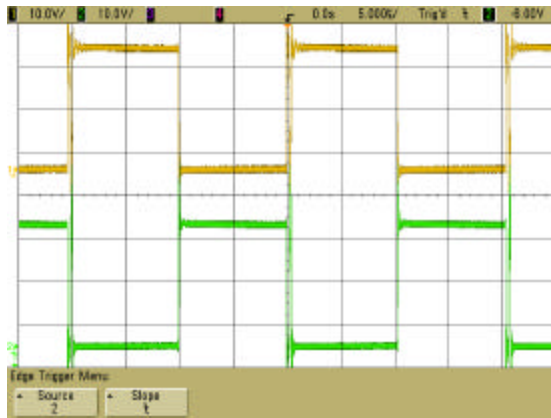
The Bridge

First, describing the MSK4225, it consists of two sets of two MOSFETs, each in a half bridge configuration. The top of each half bridge is connected to the V+ pins. The output of each half bridge is designated MOTOR A and MOTOR B. The bottom of each half bridge is designated R SENSE A and R SENSE B, respectively. They are labeled R SENSE because they are designed to be connected through external sense resistors to the system ground. It is important that the sense resistors are non-inductive types for two reasons. First, the measured current waveform will be truest when measured through a pure resistance. Secondly, the gate drive current for each MOSFET at the bottom of each half bridge has to go through the sense resistor and return to system ground. A non-inductive resistor will have the least effect on the MOSFET gate drive waveform. Inductive resistors here can actually cause enough problems and distortion of the gate signal that it can damage the transistor, so it is important to select these resistors carefully. There are high frequency diodes across the sense resistors to serve as voltage clamps in case any voltage spikes occur to protect the gate drive.

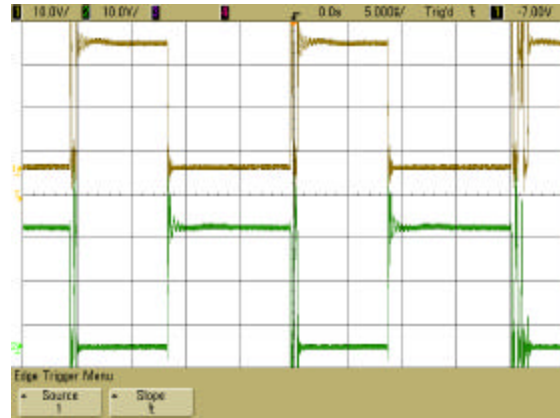
Proper bypassing and grounding of the bridge is very important. The bridge is being pulse-width modulated at 45 kHz. There are some very quick transitions of both voltage and current going on at a very high PWM rate. Any stray inductance will distort the transitions, cause voltage transients, and generally cause problems with the operation of the system. The 460uF capacitor is the bulk capacitance necessary for providing the quick current pulses demanded by the bridge. The 6.8uF polypropylene capacitor suppresses higher frequency transients and current spikes and the 0.1uF capacitor suppresses any very high frequency noise still present. It can be looked at that the three capacitors work on three different frequency ranges to keep the system as noise free as possible.

Grounding is just as important as the bypass capacitors are. Stray inductances will take away from the quick transition capability of the transistor switching function. Stray inductances will also add large voltage spikes and can actually exceed the voltage range of the bridge even with a 12v system if not careful. A ground plane, proper close placement of the capacitors and short leads from the V+ and Ground connections will go a long way to averting enough stray inductance to cause problems.

The snubber circuit created by the 100-ohm resistor and 1000-pF capacitor serves to suppress transients present on the output of the bridge. These values may have to change as the system changes with various loads. Snubber design is beyond the scope of this note, but many sources of information are available on both the web and in various texts.



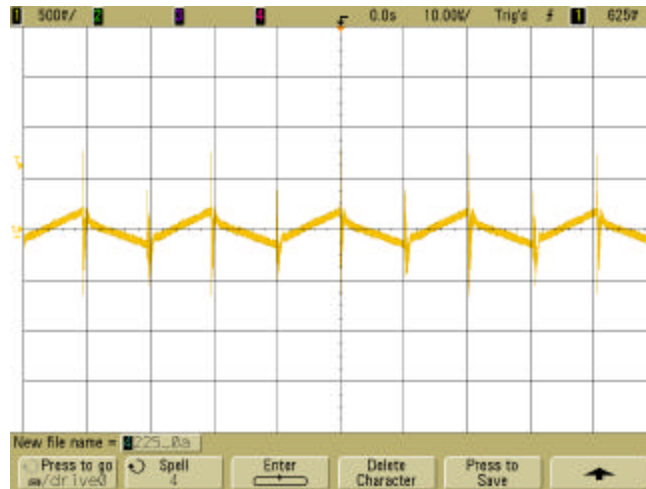
Bridge outputs at zero amps.
50% duty cycle.



Bridge outputs at 10 amps, with a
Corresponding shift in duty cycle.

Current Amplifier

The current amplifier section consists of two non-inductive, 4-wire sense resistors and a differential operational amplifier. In complimentary mode PWM switching, current is always flowing through one of the two half bridges at all times. Placing one sense resistor at the bottom of the whole half bridge will always sense current magnitude but will not provide bipolar measurements for directional information. To complete a true current loop, both magnitude and direction of current through the load is necessary for correct feedback information. Sensing the current at the bottom of each half bridge allows the separation of current through each half bridge. The voltage developed across both sense resistors are put into a differential amplifier, with one of the resistor voltages put into the non-inverting input and the other voltage put into the inverting input. The sum / difference of the two create the actual current waveform that is flowing through the load. Because the sense resistors are very low resistance to keep power dissipation low, the voltage developed across them is small. The differential amplifier has a gain of ten to help amplify the voltage for the next stage, the error amplifier.



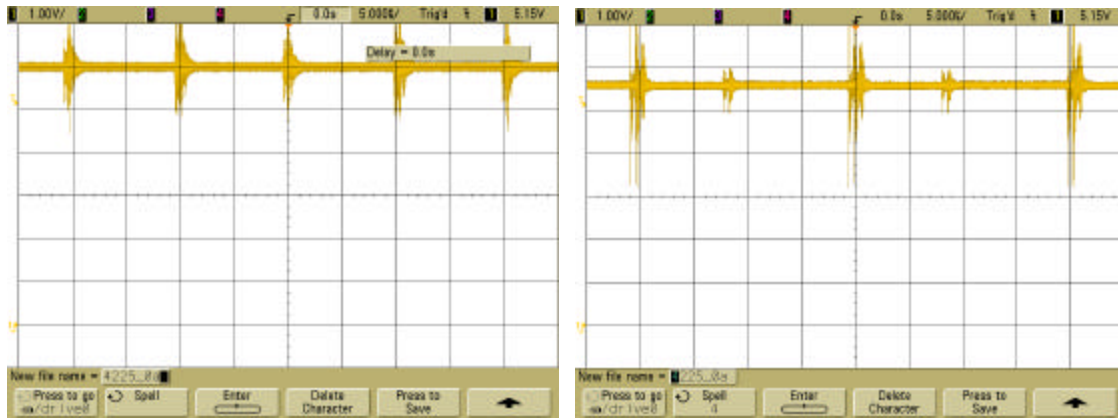
Current Waveform, U1 pin 1

Since the card has 0.010 ohm sense resistors, there is little difference in current signal as viewed on a scope between zero current and 10 amps.

Error Amplifier

The error amplifier, as set up on the evaluation board, is the other half of the LM6142 integrated circuit. It is set up so that both the command input (I Command In) and the feedback input are brought into the summing junction of the amplifier. The reason for this is that any changes in impedance due to the error amplifier output will be identical for both inputs. The voltage (current) feedback signal is set up to be the opposite polarity to the command input, so that negative feedback is achieved.

The feedback network is set up as a single pole, integrating feedback network. The resistor sets up the mid-band gain, and the combination of resistor and series capacitor compensate for the inductance and resistance of the load. Determining the values of the feedback network for each application is beyond the focus of this application note. Further information can be obtained by reviewing the Application Note titled, “Feedback Network Design.” The output of the error amplifier network feeds into the INPUT of the MSK4225, and controls the PWM duty cycle to produce current in one direction or the other.



Error amplifier at zero amps

Error amplifier at 10 amps

The scope traces for the error amplifier show 6 volts at zero current, which is exactly in the middle of the PWM range of the device. As current command increases, the error amplifier needs to compensate for that by shifting the PWM duty cycle accordingly. As is shown here, the error amplifier output voltage has decreased from the 6 volt level at zero current, forcing a shift in the duty cycle.

Transconductance

Transconductance, also known as **mutual conductance**, is a property of certain electronic components. It is the reciprocal of resistance and transconductance and is the ratio of the current at the output, Motor A and Motor B, and the voltage at the current command input, I Command In.

If +1V DC is applied to I Command In, that voltage will be compared to the result of the current amplifier stage. 10A (average current) flowing through the sense resistors will develop 0.1V (average) into the input of the current amplifier stage. That stage has a gain of 10, so 1V (average, negative, because it is a negative feedback signal) will be presented to the input of the error amplifier. The output of the error amplifier will output whatever voltage is necessary to satisfy the sum of those two signals at the input and canceling them out, making the sum 0V. This results in an overall transconductance gain of 10; 1V input creates 10A out.

MSK4225 Input Stage

The output of the error amplifier stage goes into the Input of the MSK4225. There, the voltage is compared in a comparator to a triangle wave generator. The peaks of the generator are 3V and 9V, with a frequency of 45 kHz. The result will be a pwm waveform that controls the four gate drivers for the MOSFET output stage. The error amplifier will control the PWM duty cycle to cause an average current to flow out of Motor A, through the load, and into Motor B, or vice-versa, depending on the polarity of the I Command Input. 0V of I Command Input will cause a 50% duty cycle PWM waveform to be produced at both Motor A and Motor B. Current will flow into the load one way during one half of the duty cycle, and current will flow the opposite way into the load during the other half of the duty cycle. The average of this current flow will be 0A. This method of PWM modulation is known as complimentary or locked anti-phase modulation.

For the controller to be in control, it has to be producing a PWM waveform. This is how the controller maintains control. Without PWM at the output, the controller has no way of controlling the current through the load anymore. Therefore, 100% duty cycle at either Motor A or Motor B is not a valid state for this controller to be in control. Conversely, there is no 0% duty cycle, either, as that means there would have to be 100% at the other output due to the definition of complimentary modulation. If the controller is forced to 100% duty cycle, the current flow through the load will only be limited by the resistance of the load, which may be very high in the case of a low impedance winding. The maximum supply voltage for the load must be higher than the highest voltage needed at the load because of the limitation and inherent inability of this control scheme to go to 100%.

There is no separate current limit circuit in this evaluation board design, so duty cycle extremes need to be avoided. If current limiting is needed, some sort of clamping network would have to be devised to limit the voltage at the error amplifier, resulting in a clamped duty cycle limit. Or, the output of the current amplifier compared to a current limit reference using a comparator that is fed into the DISABLE pin on the MSK4225.